# DieCORE™ MSS IP

## 112Gbps XSR Low-Power SerDes

### About AlphaWave

AlphaWave IP is a leading provider of DSP based silicon IP and chiplet solutions targeted for **Data Processing** (Datacenter/Compute) and **Data Generation** (Optic/Retimer) and **Data Storage** (SSD/Flash)

### Management Team

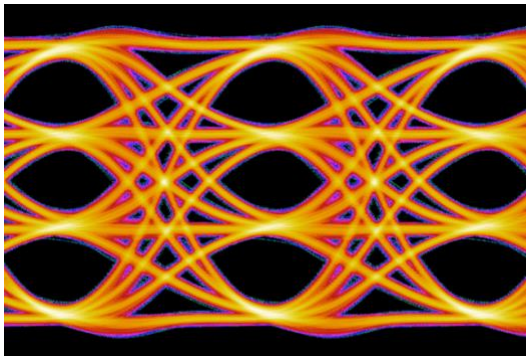
Founded by a team of leading technologists and Silicon Valley entrepreneurs, all with a history of building successful silicon IP businesses and technologies to drive next generation connectivity

### Execution Status

- **2018:** First AlphaCORE™ TSMC N7 Silicon is back
- **2019:** AlphaCORE™ N7 IP in production and AlphaCORE™ ported to TSMC N5
- **2020:** Taped out production version of AlphaCORE™ in N6 and N5

## *DieCORE™ IP Highlights*

- High Speed Performance
  - DieCORE employs a low noise, high speed analog front end to support both PAM4 and NRZ signalling up to 112Gbps
- Low Power Architecture
  - DieCORE operates at sub-mW/Gbps power consumption, while still providing robust 8-10dB of equalization for die-die MCMs



## *Overview*

The Alphawave DieCORE delivers the world's highest density, lowest power die-to-die connectivity solution for MCMs and interposers based on IEEE XSR/USR serial standards.

The DieCORE is a companion IP to the AlphaCORE LR IP, for large datacenter SOCs that are moving to multi-chiplet MCM products based on organic substrates or Silicon interposers.

## *Leading Edge IO Density*

The DieCORE allows signals to be transferred across chiplets with sub-mW/Gbps power consumption, and at an IO density of over 1Tbps per millimeter of Silicon

- Supports 1, 4, 8, 16 lane configurations, as well as both north/south and east/west orientations
- DieCORE also supports multiple rows of stacking flexibility

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# DieCORE™ MSS IP

## 112Gbps XSR Low-Power SerDes

### Power Consumption

Power optimized, short reach architecture consumes for 112G XSR standards

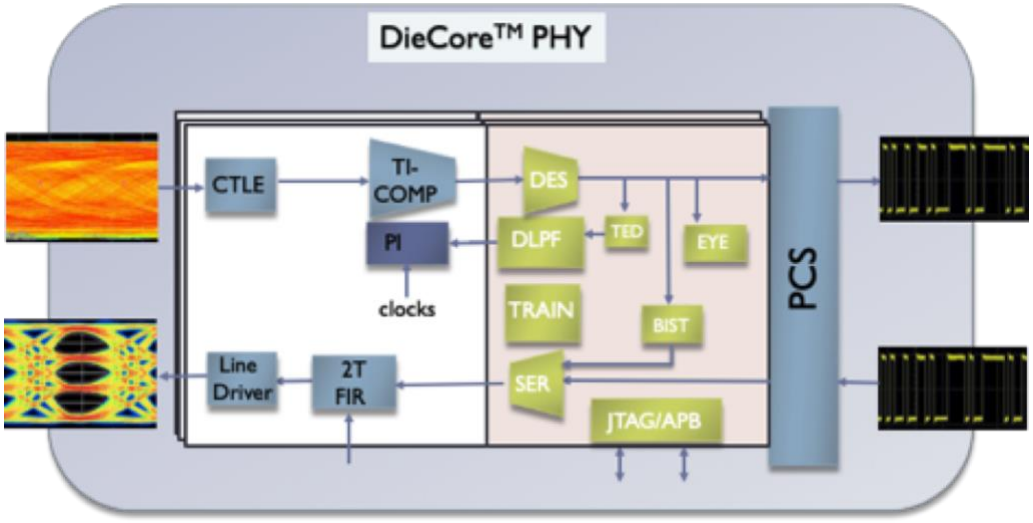
### Area Consumption

The DieCORE™ MSS IP delivers greater than 1Tbps of IO bandwidth density per millimeter of silicon IO. The DieCORE™ IP is available in 1/4/8 or 16 lane configurations, as well as both N/S and E/W orientations

### Target Channels

Innovative low power architecture supports eXtra Short Reach (XSR) channel losses up to 10dB for System on Package solutions.

## DieCORE™ Features




- The DieCORE™ MSS IP employs a high speed analog front end that intergates analog equalization for channels up to 10dB of loss at 112Gbps
- The DieCORE™ CDR employs a wide tuning, tracking CDR that can track hundreds of ppm frequency error and provide continuous tracking of data
- The DieCORE™ Master Controller integrates and simplifies analog and equalization training, while maintaining product level flexibility and workarounds
- DieCORE eliminates the need for costly proprietary interface solutions by delivering high density low power support for both XSR and USR IEEE and OIF standards

## Key Specifications

| Parameter | Design Specification |
|---|---|
| Receive Equalization | Designed for XSR/VSR based systems up to 10dB of insertion loss at Nyquist for PAM4<br>Includes blind adaptive receive equalizer |
| Output Driver Voltage | Programmable 200 – 600 mVdiff-pkpk |
| Supply Voltages | Core - 0.75V<br>IO - 1.2 V |
| Devices Used | Core – SVT, LVT and ULVT<br>IO - 1.8V SVT |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