



AlphaCORE™ MSS IP

I – 112Gbps DSP Multi-Standard SerDes

About AlphaWave

AlphaWave IP is a leading provider of DSP based silicon IP and chiplet solutions targeted for **Data Processing** (Datacenter/Compute) and **Data Generation** (Optic/Retimer) and **Data Storage** (SSD/Flash)

Management Team

Founded by a team of leading technologists and Silicon Valley entrepreneurs, all with a history of building successful silicon IP businesses and technologies to drive next generation connectivity

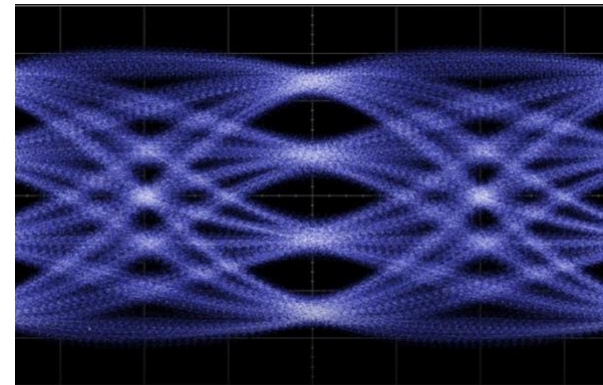
Execution Status

- **2018:** First AlphaCORE™ TSMC N7 Silicon is back
- **2019:** AlphaCORE™ N7 IP in production and AlphaCORE™ ported to TSMC N5
- **2020:** Taped out production version of AlphaCORE™ in N6 and N5



AlphaCORE™ IP Highlights

- Low power, register configurable architecture operates continuously from 1.0625Gbps to 112Gbps
- Dynamic architecture can support all modern Data Center standards such as Ethernet, PCIe and CPRI
- Low power DSP architectures



Overview

The Alphawave AlphaCORE™ DSP PHY IP is a high-performance, low-power, Multi-Standard SerDes (MSS) IP. It is a highly configurable IP that supports all leading edge NRZ and PAM data center standards from 1Gbps to 112Gbps, ranging from protocols such as PCI-Express Gen1-5 through to 10G/25G/56G/112Gbps Ethernet.

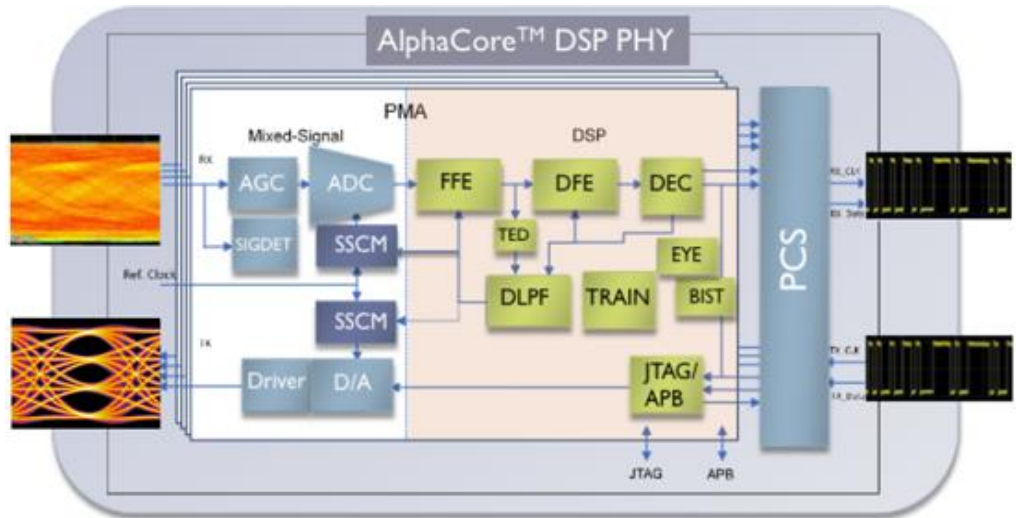
Configurability

The brilliance of the Alphawave AlphaCORE™ DSP PHY IP is in its patented, register configurable DSP architecture. The AlphaCORE™ leverages high performance A/D converters to digitize incoming data over copper or fiber. The AlphaCORE™ DSP Master Controller uses patented signal processing techniques to recover the signal, while optimizing both power and latency.

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AlphaCORE™ Features



Power Consumption

Ultra-low-power, DSP based architecture consumes for 112G PAM4 Ethernet standards

Area Consumption

The AlphaCORE DSP MSS IP delivers world leading Gbps of IO bandwidth density per millimeter of silicon IO. The AlphaCORE™ IP is available in 1/2/4/8 or 16 lane configurations, as well as both N/S and E/W orientations

Target Channels

Innovative ADC and DSP architecture supports long reach channel losses up to 40dB PAM4 with no Near-End Crosstalk (NEXT) and up to 36dB with NEXT. The AlphaCORE™ MSS also supports short-reach, high bandwidth interfaces to fiber interconnects. AlphaCORE™ power can be optimized for both shorter channels and lower data rates

- The AlphaCORE™ MSS IP employs a high speed A/D architecture that has configurability for both the A/D sampling rate as well as the A/D resolution
- The AlphaCORE™ CDR employs a wide tuning, sub-sampling clock multiplier that can track over 5000ppm error for both scrambled and 8B/10B encoded data
- The AlphaCORE™ DSP Master Controller includes:
 - All required training is integrated, without the need of external RAM
 - Non-destructive eye monitoring
 - 1+D Partial Response Coding
- PCIe Gen1-5 PCS layer, Ethernet Link Training and Auto-Negotiation layer also available

Key Specifications

Parameter	Design Specification
Receive Equalization	Designed for closed eye, backplane systems up to 36dB of insertion loss at Nyquist for PAM4 and greater than 40dB of loss for NRZ with NEXT Includes blind adaptive equalizer and channel estimator
Output Driver Voltage	Programmable 400 – 1200 mVdiff-pkpk (inner eye)
Supply Voltages	Core - 0.75V IO - 1.2V
Devices Used	Core – SVT, LVT and ULVT IO - 1.8V SVT